a configuration step in which the memory system is set up by means of control commands associated with the set of input data and the set of output data; and

an execution step in which, on the basis of the control commands, the memory system:

selects a first memory circuit and generates a write-address for the first memory circuit for a data belonging to the set of input data;

selects a second memory circuit and generates a read-address for the second memory circuit for a data belonging to the set of output data.

REMARKS

Claims 1-5 remain pending in this application and have been amended to attend to matters of form. Claims 1, 4 and 5 are the independent claims. Favorable reconsideration is respectfully requested.

In the Office Action, Claims 1-5 were objected to because of informalities. As shown above, all the claims have been carefully reviewed and amended to attend to the points raised in the Office action. Withdrawal of the objection is respectfully requested.

Claims 1-5 were rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent 4,734,850 (Torii et al.)

Applicant respectfully submits that the rejected claims as amended are patentable for at least the following reasons.

Claim 1 as amended is directed to a data processing arrangement including a first processor for providing successive sets of input data, a second processor for receiving successive sets of output data, and a memory system including a plurality of memory circuits for receiving the successive sets of input data from the first processor and providing the successive sets of output data to the second processor. The data processing arrangement also includes a master controller for setting up the memory system using control commands associated with a set of input data and a set of output data; and a control unit for, on the basis of the control commands, selecting a first memory circuit and generating a write-address for the first memory circuit when a data from the set of input data is provided by the first processor, and for, on the basis of the control commands, selecting a second memory circuit and generating a read-address in the second memory circuit when a data from the set of output data is required by the second processor.

As understood by Applicant, Torii et al. relates to a data process system that includes plural storage means each capable of concurrent and intermediate reading and writing of a set of data signals.

The Office Action cites to Fig. 2 and element 41 (mode indicating ckt) as providing a signal for repetitively indicating

at a constant interval a write mode to banks 47 and 48. Applicant notes, however, that Fig. 2 of Torii et al. is directed to a single FIFO memory as shown in Fig. 1. In particular, while Fig. 1 shows three FIFO memories 20, 21 and 22, Fig. 2 only shows a block diagram of only one FIFO (see col. 2, lines 64-66).

Applicant points this out because the Mode Indicating Ckt 41 only controls one FIFO memory not all the FIFO memories. Claim 1 recites a master controller for setting up the memory system. It is believed clear that the Mode Indicating Ckt 41 does not set up all the FIFO memories 20, 21 and 22 in Torii et al. and does not show the master controller as recited in Claim 1.

Since it is well settled that an anticipatory reference must show each and every feature as recited in a claim, the Section 102 rejection of Claim 1 is believed improper.

Independent Claims 4 and 5 recite similar features as recited in Claim 1, and are believed allowable for at least the same reason.

A review of the other art of record has failed to reveal anything which, in Applicant's opinion, would remedy the deficiencies of the art discussed above, as references against the independent claims. Those claims are therefore believed patentable over the art of record.

The other rejected claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the same reasons.

In addition, however, each dependent claim is also deemed to define an additional aspect of the invention, and should be individually considered on its own merits.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

Applicant's undersigned attorney may be reached by telephone at the number given below.

Respectfully submitted,

By _____
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CERTIFICATE OF MAILING

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On July 2, 2001

By Elissa DeLucay

Appendix of Marked-up Claims

1. (Amended) A data processing arrangement [(1)] comprising:

[-] a first processor [(PROC1)] for providing successive sets of input data;

[-] a second processor [(PROC2)] for receiving successive sets of output data;

[-] a memory system [(2)] comprising a plurality of memory circuits [(MEM)] for receiving the successive sets of input data and providing the successive sets of output data[,]; [wherein]

[- the data processing arrangement further comprises] a master controller [(MCP)] for setting up the memory system [by means of] using control commands [(CC)] associated with a set of input data and a set of output data; and

[the memory system further comprises] a control unit [(MCU):][-] for, on the basis of the control commands, selecting a first memory circuit and generating a write-address [(AD_W) in said] for the first memory circuit when a data [(Di)] from the set of input data is provided by the first processor, and [:] [-] for, on the basis of the control commands, selecting a second memory circuit and generating a read-address [(AD_R)] in [said] the second memory circuit when a data [(Do)] from the set of output data is required by the second processor.

2. (Amended) A data processing arrangement, as claimed in claim 1, wherein the control unit comprises:

[-] a write-counter [(CNT_W)] whose value is modified in association with [a] the data received from the set of input data and which value indicates the write-address of the data in [said] the first memory circuit; and

[-] a read-counter [(CNT_R)] whose value is modified in association with [a] the data provided from the set of output data and which value indicates the read-address of the data in [said] the second memory circuit.

3. (Amended) A data processing arrangement, as claimed in claim 1, wherein the control unit comprises a write-input port [(7)] for receiving a write-data signal [(NXT_W)] from the first processor in response to which the control unit generates the write-address and the control unit further comprises a read-input port [(8)] for receiving a read-data signal [(NXT_R)] from the second processor in response to which the control unit generates the read-address.

4. (Amended) A memory system [(2)] comprising:

a plurality of memory circuits [(MEM)] for receiving successive sets of input data and for providing successive sets of output data[, wherein the memory system further comprises];

a control unit [(MCU)] being programmable by means of control

commands [(CC)] associated with a set of input data and a set of output data and, on the basis of these control commands, for selecting a first memory circuit and generating a write-address [(AD_W) in said] for the first memory circuit, when a data [(Di)] from the set of input data is received, and for selecting a second memory circuit and generating a read-address [(AD_R) in said] for the second memory circuit, when a data [(Do)] from the set of output data is provided.

5. (Amended) A method of processing data in a data processing arrangement [(1) comprising:-] including a first processor [(PROC1)] for providing successive sets of input data[; -], a second processor [(PROC2)] for receiving successive sets of output data[;] and [-] a memory system [(2) comprising] including a plurality of memory circuits [(MEM)] for receiving the successive sets of input data and providing the successive sets of output data,

[wherein] the method [comprises] comprising, for a set of input data and a set of output data, the following steps:

[-] a configuration step in which the memory system is set up by means of control commands associated with the set of input data and the set of output data; and

[-] an execution step in which, on the basis of the control commands, the memory system:

[-] selects a first memory circuit and generates a write-

address [in] for the first memory circuit for a data belonging to the set of input data;

[-] selects a second memory circuit and generates a read-address [in] for the second memory circuit for a data belonging to the set of output data.